Pixel Design of Gain-Boosted Event-Based Vision Sensor to Control Event Noise and Latency at Low Illuminance

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Abstract – Event-based vision sensor (EVS) generally faces issues with false detection, commonly known as the background rate (BGR), because of pixel noise, especially in the case of low illuminance. Previous studies have shown that EVS pixel noise depends on the specific parasitic capacitance and bias current in logarithmic EVS pixels. However, studies providing pixel design guidelines for controlling BGR in the more advantageous gain-boosted EVS pixels are limited. Therefore, we aim to develop a guideline for pixel design by proposing a method for controlling the BGR. This approach involves adjusting the specific parasitic capacitance in gain-boosted EVS pixels. In addition, we show the measurement results demonstrating the validity of this method.

I. Introduction

Event-based vision sensor (EVS) is specialized sensor that detects changes in brightness, providing low power consumption and high-speed detection advantages [1-4]. However, EVS faces a significant challenge with noise events, commonly referred to as the background rate (BGR), which is primarily caused by pixel noise at low illuminance [4-7]. Figure 1 shows an example of the illuminance dependence of BGR [4]. The BGR is undesirable because it leads to increased output data volume [8]. Previous studies have described how to control EVS pixel noise by optimizing the bias current [7]. Other studies have shown that EVS characteristics depend on parasitic capacitance in the pixel based on physical models [9,10,11]. These studies are based on the logarithmic EVS pixel shown in Figure 2. In the reference [12], a gain-boosted EVS is proposed as another pixel configuration for EVS shown in Figure 3. Gain-boosted EVS has a high current–voltage conversion gain and superior EVS characteristics. However, studies providing pixel design guidelines for controlling BGR in the gain-boosted EVS pixels are limited. This study proposes a method for controlling the BGR and latency by appropriately adjusting the specific parasitic capacitance in the gain-boosted EVS pixel. Furthermore, we show the measurement results that demonstrate the validity of the method.

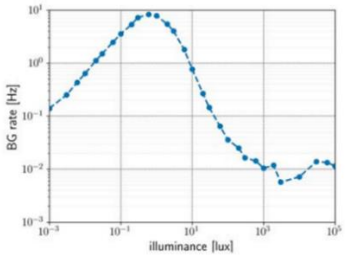

Figure 1. Measurement results of event noise (background rate) vs illuminance

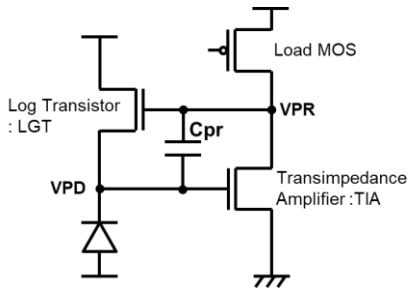

Figure 2. Schematic of the logarithmic EVS pixel

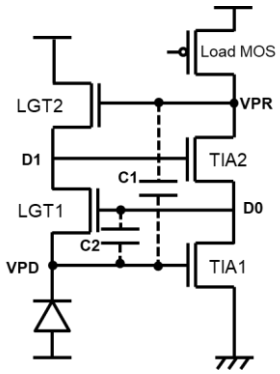

Figure 3. Schematic of the gain-boosted EVS pixel

II. Experiments

This study was conducted in the following order.
1. We investigated the dominant noise factor based on the logarithmic EVS in Figure 2.
2. We derived the parameters controlling the dominant noise component.
3. We extended the concept to the gain-boosted EVS in Figure 3.
4. We prepared some samples and confirmed the validity of the approach by measurements.

1. Dominant factors of pixel noise

At low illuminance, the current generated at the photodiode is very small, and the log transistor (LGT) of the logarithmic EVS shown in Figure 2 operates in the subthreshold region. The driving current of the LGT at low illuminance is generally several orders of magnitude smaller than that of the transimpedance amplifier (TIA). Therefore, the LGT noise is considered the dominant component of pixel noise. Figure 4 shows the results of an analysis of transistor noise at low illuminance obtained using SPICE Sim. This figure shows that LGT thermal noise is the dominant component in the logarithmic EVS pixel. In principle, LGT thermal noise can be improved by increasing the photocurrent. However, increasing the photocurrent is difficult because the photocurrent is limited by the size of the photodiode and the illuminance on the sensor surface. Therefore, optimizing the LGT noise by controlling the bandwidth is necessary.

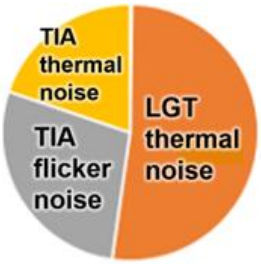

Figure 4. The contribution of each transistor noise in the EVS pixel, as shown in Figure 2, obtained using SPICE Sim

2. Parameters controlling the LGT noise

The bandwidth of the logarithmic EVS pixel has been investigated [9, 10, 11]. These studies focused on the capacitance between the input and output of the logarithmic EVS pixel, which corresponds to C_{pr} in Figure 2. In this study, we prepared a pixel circuit model that includes the LGT noise $\boldsymbol{I_{n\_LGT}}$, as shown in Figure 5, to clarify the capacitance controlling the bandwidth of the LGT noise. The following two equations can be derived from this pixel circuit model:

$$g_m(V_{PR} - V_{PD}) + I_{n\_LGT} - sV_{PD}C_{pd} - sC_{pr}(V_{PD} - V_{PR}) = 0 \quad (1)$$

$$G_m V_{PD} + sV_{PR}C_o + \frac{V_{PR}}{R_o} + sC_{pr}(V_{PR} - V_{PD}) = 0 \quad (2)$$

The parameters in the formula are defined as follows:

$\boldsymbol{g_m}$	Transconductance of LGT
$\boldsymbol{G_m}$	Transconductance of TIA
$\boldsymbol{I_{n\_LGT}}$	Noise of LGT
$\boldsymbol{V_{PR}}$	Output node voltage of pixel
$\boldsymbol{V_{PD}}$	Input node voltage of pixel
$\boldsymbol{C_{pr}}$	Capacitance between the input and output
$\boldsymbol{C_{pd}}$	Total capacitance of the input node excluding C_{pr}
$\boldsymbol{C_o}$	Total capacitance of the output node excluding C_{pr}

From these equations, the relationship between LGT noise $\boldsymbol{I_{n\_LGT}}$ and output voltage $\boldsymbol{V_{PR}}$ can be formulated as follows:

$$\frac{V_{PR}}{I_{n_{LGT}}} = -\frac{\dfrac{sC_{pr} - G_m}{(C_oC_{pr} + C_oC_{pd} + C_{pd}C_{pr})}}{s^2 + \dfrac{\left(G_mC_{pr} + g_mC_o + \dfrac{C_{pd}+C_{pr}}{R_o}\right)}{(C_oC_{pr} + C_oC_{pd} + C_{pd}C_{pr})}s + \dfrac{g_m(1 + G_mR_o)}{R_o(C_oC_{pr} + C_oC_{pd} + C_{pd}C_{pr})}} \quad (3)$$

Assuming that the LGT $\boldsymbol{g_m}$ is sufficiently smaller than the TIA $\boldsymbol{G_m}$ at low illuminance, the cutoff frequency of the LGT noise can be calculated as follows:

$$\omega \approx \frac{g_m}{C_{pr} + \dfrac{C_{pd}}{(1 + G_mR_o)}} \approx \frac{g_m}{C_{pr}} \quad (4)$$

The equation is simplified by assuming that $\boldsymbol{G_mR_o \gg 1}$. Equation (4) shows that C_{pr} appears to be larger than C_{pd} by the gain of the TIA. Therefore, C_{pr} contributes significantly to the noise band of the LGT. This is commonly called the Miller effect.

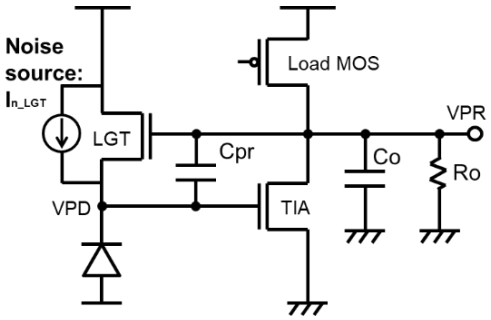

Figure 5. EVS pixel circuit model incorporating LGT noise

3. Extending the concept to the gain-boosted EVS

Gain-boosted EVS pixels, which have a large current–voltage conversion gain and superior characteristics, are often used for EVS. Figure 6 shows the contribution rate of each transistor noise at low illuminance analyzed using SPICE Sim for a gain-boosted EVS. From Figure 6, the dominant component is the thermal noise of LGT1. Therefore, controlling the noise band of LGT1 is beneficial. The parameter C_{pr}, which controls the noise band of LGT1, can be defined as follows:

$$C_{pr} \approx C_1 + \frac{C_2}{2} \quad (5)$$

Equation (5) is defined, considering the difference in the Miller effect between C_1 and C_2. This implies that the coefficients are determined by considering that C_1 has two gain stages, TIA1 and TIA2, and C_2 has one gain stage, TIA1. By appropriately adjusting the C_{pr}, the noise band of LGT1, which corresponds to the BGR, can be controlled. We demonstrate the validity of this concept, by preparing samples with different C_{pr}. This involves changing the layout of the 4.86-μm-pitch gain-boosted EVS pixel. Subsequently, we measure the correlation between C_{pr} and the BGR.

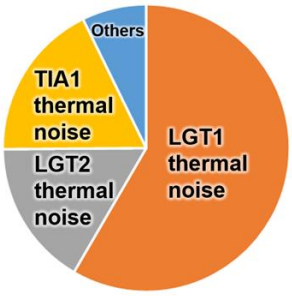

Figure 6. The contribution of each transistor noise in the gain-boosted EVS pixel (shown in Figure 3). This result is obtained using SPICE Sim

III. Results and Discussion

This section discusses the results of the BGR measurements and proves the validity of the proposed method. Figure 7 shows the correlation between the BGR at 0.3 lux and the C_{pr} defined as $C_1 + C_2 / 2$ for the gain-boosted EVS. The results indicate an exponential relationship between the BGR and C_{pr}, thereby validating our hypothesis that the BGR of gain-boosted EVS can be controlled by adjusting the C_{pr}. In addition, the C_{pr} influences the time constant of the VPD node, which affects the latency at low illuminance. The VPD is the input node of the gain-boosted EVS shown in Figure 3. Figure 8 shows the correlation between latency and the BGR at 0.3 lux. The latency in Figure 8 is the time from illuminance change to a positive event output when a 2x contrast change occurs at 0.3 lux. This result reveals a trade-off between these two characteristics; designing a larger C_{pr} improves the BGR but worsens latency. Determining the optimal C_{pr} is crucial, considering this trade-off in gain-boosted EVS pixel design. Figure 9 shows the layout for the 4.86-μm-pitch gain-boosted EVS pixel. In this layout, the C_{pr} is optimally adjusted so that both the BGR and latency meet the required characteristics. Figure 10(b) shows an image captured by the EVS prepared in this study.

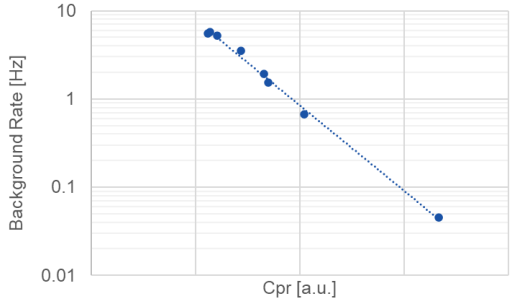

Figure 7. BGR vs. Cpr design value defined as $C_1 + C_2 / 2$ at 0.3 lux

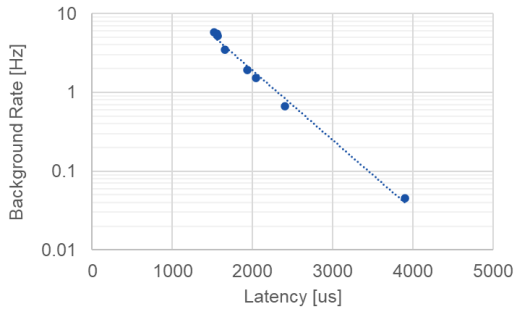

Figure 8. Trade-off relation between latency and the BGR at 0.3 lux

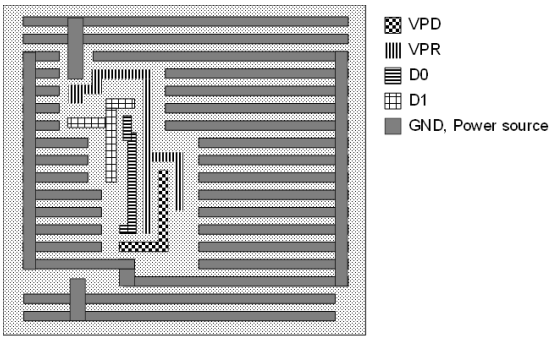

Figure 9. Layout example for a gain-boosted EVS pixel. The C_{pr} is optimally adjusted so that both the BGR and latency meet the required characteristics.

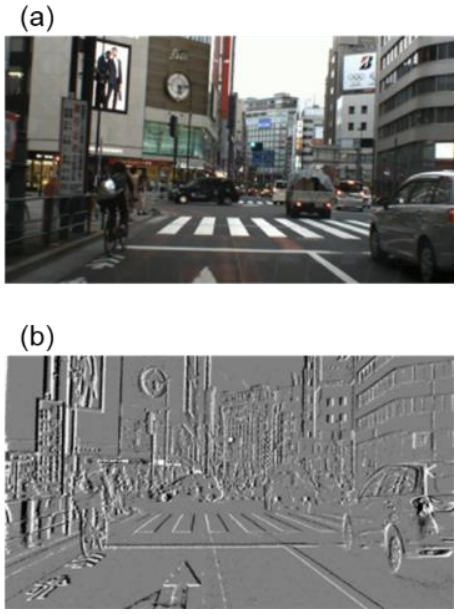

Figure 10. (a) Image captured using a normal CMOS image sensor. (b) Image captured by using the EVS prepared in this study.

IV. Conclusion

In this study, we defined the C_{pr} for a gain-boosted EVS pixel, which controls the BGR at low illuminance. By preparing several samples with different C_{pr} designs, we obtained measurement results demonstrating the validity of our C_{pr} definition. We also presented the layout for a gain-boosted EVS pixel designed to meet both the required BGR and latency by optimizing the C_{pr}.

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